Timers

Timerların periyodik kesme, PWM gibi periyodik sinyaller üretme ve belirli zaman bekleme gibi kullanım alanları vardır.
STM32F4 mikrokontrolcüsünde 3 çeşit timer vardır.

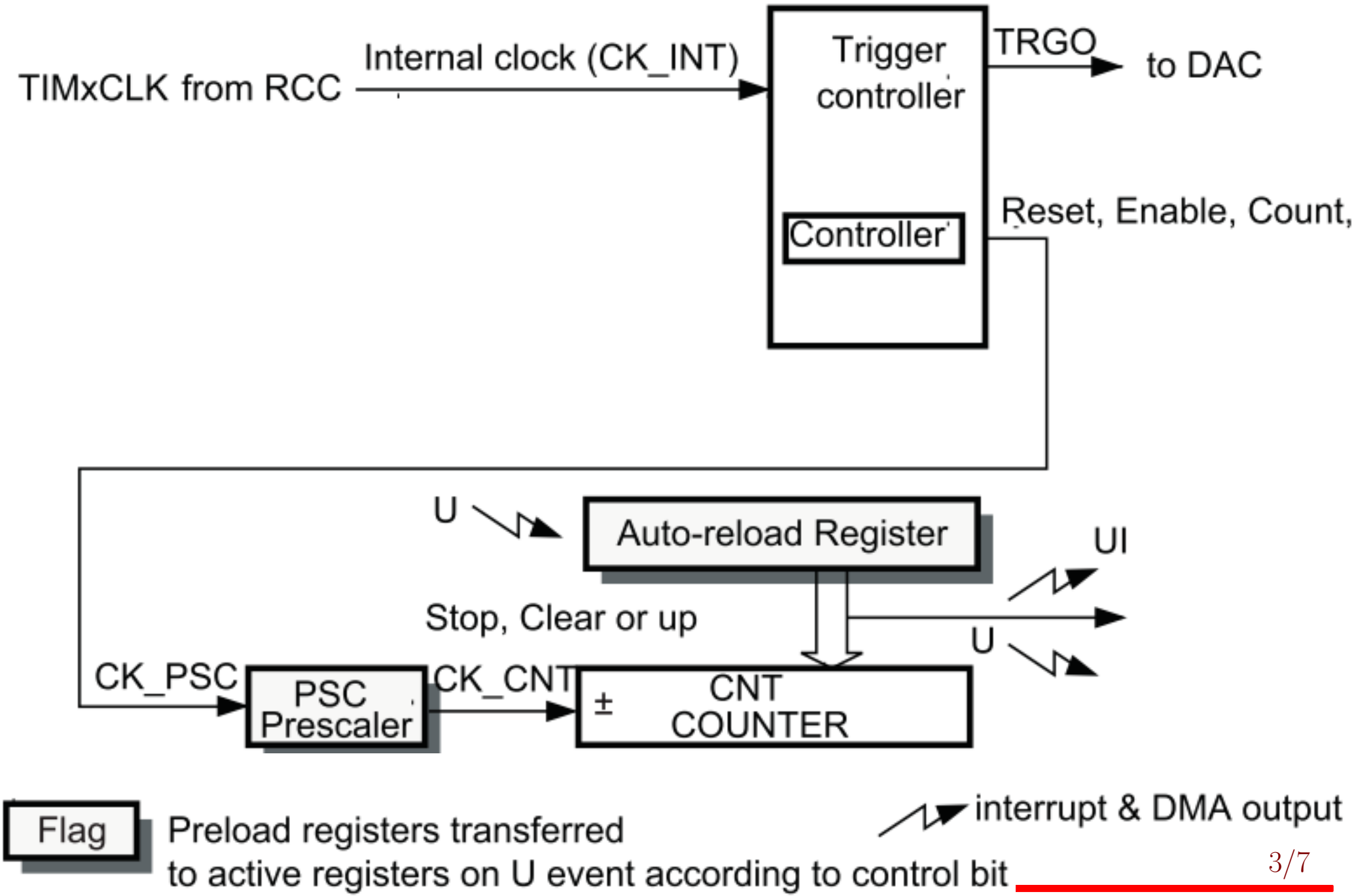
- TIM6, TM7: Temel Timer
- TIM2-TIM5, TIM9-TIM14 : Genel Amaçlı Timer:
- TIM1, TIM8: Gelişmiş Kontrollü Timer

Basic Timers: TIM6, TIM7

Temel zamanlayıcı (TIM6 ve TIM7) özellikleri şunları içerir:

- 16-bit otomatik yeniden yükleme sayacı (Auto Reload)
- 16-bit programlanabilir ön ölçekleme sayacı (Prescaler)
- Güncellemede (sayaç taşması - overflow- sayma işleminin bitmrsi) Interrupt / DMA (Kesme / Direct Memory Access) yapılabilir.

Basic Timers: TIM6, TIM7



Basic Timers: TIM6, TIM7

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TIM6 and TIM7 control register 1 (TIMx_CR1)

Address offset: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ARPE	Reserved			OPM	URS	UDIS	CEN
								rw				rw	rw	rw	rw

Bit 7 **ARPE**: Auto-reload preload enable

0: TIMx_ARR register is not buffered.

1: TIMx_ARR register is buffered.

Bit 0 **CEN**: Counter enable

0: Counter disabled

1: Counter enabled

Basic Timers: TIM6, TIM7

TIM6 and TIM7 DMA/Interrupt enable register (TIMx_DIER)

Address offset: 0x0C

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							UDE	Reserved							UIE
							rw								rw

Bit 0 **UIE**: Update interrupt enable
0: Update interrupt disabled.
1: Update interrupt enabled.

TIM6 and TIM7 status register (TIMx_SR)

Address offset: 0x10

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															UIF
															rc_w0

Bit 0 **UIF**: Update interrupt flag
This bit is set by hardware on an update event. It is cleared by software.
0: No update occurred.
1: Update interrupt pending. This bit is set by hardware when the registers are updated:

Basic Timers: TIM6, TIM7

TIM6 and TIM7 counter (TIMx_CNT)

Address offset: 0x24

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 **CNT[15:0]**: Counter value

TIM6 and TIM7 prescaler (TIMx_PSC)

Address offset: 0x28

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 **PSC[15:0]**: Prescaler value

The counter clock frequency CK_CNT is equal to f_{CK_PSC} / (PSC[15:0] + 1).

PSC contains the value to be loaded in the active prescaler register at each update event

Basic Timers: TIM6, TIM7

TIM6 and TIM7 auto-reload register (TIMx_ARR)

Address offset: 0x2C

Reset value: 0xFFFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 **ARR[15:0]**: Auto-reload value

ARR is the value to be loaded into the actual auto-reload register.